CURRICULUM VITAE

SURNAME AND NAME	**Michele Portolan**
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E-mail address	**michele.portolan@grenoble-inp.fr**
Nationality	**Italian**
Birth date	**9 July 1979**

Academic Position (if the candidate holds a position in a University)

Qualification/Title	**Associate Professor**
University	**Grenoble-INP**
Department	**Phelma**
Academic Field	**Electronics Engineering**
Academic Discipline	**Digital Design, Design For Test, Fault Tolerance, Embedded systems**

Working experience (please use the following table in order to briefly describe the working positions covered by the candidate)

Dates (from .. to..)	**September 2013-Present**
Name and address of the Employer (Public or/and private institution/body)	**Grenoble-INP, (Public University)**
Position held (for positions in Universities, the candidate should indicate the Faculty/College/School and the Department)	**Associate Professor at PHELMA School of Physics, Electronics and Material Engineering**
Main activities/responsibilities	**Responsible of the "Embedded Systems and Software" major (SLE in French) from 2013, which became "Embedded Systems and Connected Objects" (SEOC in French) in September 2°17, both common with the ENSIMAG School of Computer Science.** **Assured a mean of 300+ teaching hours per year.** **One of the main actors for the NXP-Phelma partnerships signed in 2017.**

Dates (from .. to..)	**January 2011-August 2013**
Name and address of the Employer (Public or/and private institution/body)	**Alcatel-Lucent Bell Labs France (private R&D body)**

Position held (for positions in Universities, the candidate should indicate the Faculty/College/School and the Department)	**Member of Technical Staff**
Main activities/responsibilities	**Inside the "Triple-Play Wireless Networks team", my role was to investigate the impact of 4G cloud-based solutions on Alcatel-Lucent's Radio Access Network (RAN) infrastructure. In particular, I worked on the deployment of a research prototype based on the OpenAirInterface initiative and connected to a commercial Remote Radio Head (RRH) through an innovative and patented solution based on a hybrid CPRI/Ethernet solution.** **In parallel, I continued my activity in the IEEE P1687 standard Working Group started**

Dates (from .. to..)	**July 2007-December 2011**
Name and address of the Employer (Public or/and private institution/body)	**Bell Labs Ireland**
Position held (for positions in Universities, the candidate should indicate the Faculty/College/School and the Department)	**Post-Doc (until December 2007), Member of Technical Staff (since January 2008)**
Main activities/responsibilities	**Since my arrival, I was Alcatel-Lucent representative in the IEEE P1687 standardisation committee. My role was both observing and influencing the standard development in order to maximise its industrial impact and assure ALU's technical excellence. This allowed me to interact with some of the main deciders in the digital DfT domain and gain first-hand knowledge of a promising new technology. This resulted in several conference and journal papers, and in roughly 15-20 patent submission (100% grant rate as of September 2017).** **In accordance with the strategic evolution of Bell Labs Ireland, I also worked on 3G and 4G Small Cell automated deployment, with a particular emphasis on the deployment of genetic algorithms in field prototypes.**

Dates (from .. to..)	**September 2006-June 2007**
Name and address of the Employer (Public or/and private institution/body)	**Grenoble-INP**
Position held (for positions in Universities, the candidate should indicate the Faculty/College/School and the Department)	**Lecturer (in French ATER)**
Main activities/responsibilities	**In this role, I assured the same teaching responsibilities of an Associate Professor (~200 teachin hours) in the fields of Digital Design and Computer Science. Research-wise, I pursued my PhD work and prepared the technical hand-off of my results.**

Education and Training (please use the following table to describe Degrees awarded, by only indicating the information concerning Bachelor's Degree, Master of Science's Degree or/and PhD)

Date	**December 2016**
Institution which issued the degree	**Grenoble-INP**
Type of Degree awarded (only Bachelor's Degree, Master of Science's Degree, PhD)	**PhD in Micro and Nano Electronics. Thesis title: "Development of a Sure and Reliable SoC"**

Date	**September 2013**
Institution which issued the degree	**Politecnico di Torino**
Type of Degree awarded (only Bachelor's Degree, Master of Science's Degree, PhD)	**Laurea in Ingenieria Elettronica, 110L**

Date	**June 2013**
Institution which issued the degree	**Grenoble-INP**
Type of Degree awarded (only Bachelor's Degree, Master of Science's Degree, PhD)	**Master's Degree in Telecommunication Engineering, issued from a double degree program with the Politecnico di Torino**

EVALUATION FIELDS

1. Scientific Activity

1.1 Thanks to my seven-year activity (from 2007 to 2014) in the IEEE P1687 standardization committee, I was able to influence and get first-hand knowledge of one of the main innovations in the field of automated testing in recent years. It was also the opportunity to meet and interact with the main deciders and influencers, forging a reputation of disruptive innovation with real industry impact potential. This resulted not only in the publications presented in this paragraph, but also in an important patent portfolio which can be found in the annex. The grant rate so far is 100%, which demonstrate their innovative components.
The following three publications show the evolution of my work:

[1] Portolan M., Goyal S., Van Treuren B.,, «Executing IJTAG: Are Vectors Enough? », IEEE Design & Test, Year: 2013, Volume: 30, Issue: 5 Pages: 15 - 25, DOI: 10.1109/MDAT.2013.2278541
[2] 1687-2014 - IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device, 5 Dec. 2014, DOI: 10.1109/IEEESTD.2014.6974961
[3] Portolan M., "A novel test generation and application flow for functional access to IEEE 1687 instruments", 21th IEEE European Test Symposium (ETS), Year: 2016, Pages: 1 - 6, DOI: 10.1109/ETS.2016.7519302

Publication [1] appeared as part of a Special Issue for the upcoming 1687 standard of IEEE Design and Test, the only IEEE journal fully dedicated to test. In it, I presented a disruptive hardware-based approach for test execution that broke the traditional static vector delivery and application approach. It is the very first paper focusing on the usage of the standard rather than

on its implementation, and a precursor of an issue that is rapidly gaining momentum: it is, for instance, one of the key points of the new IEEE P1687.1 working Group launched in 2017 to extend 1687 beyond JTAG and allow access to embedded resources using arbitrary protocols. The innovation described in [1] is also the heart of 6 patents, detailed in point 1.2

Publication [2] refers to the official 1687 standard document. By its nature a standard is a group effort so I cannot claim authorships of any particular point, but in my seven-year efforts I gave a recognized contribution in guiding the discussions and shaping the final form of the standard. The standard is rapidly being adopted by the industry well beyond the initial participants, and it is presented as a "paradigm shift" that will deeply influence the field of testing in the coming years.

Publication [3] is the most recent and probably the most disruptive: building on the experience of [1] and [2], it presents a completely new software flow that breaks the traditional barrier between test generation and application, making it possible to tackle the most complex and open problems of the field. This solution is a now at the heart of the new P1687.1 standard Working Group discussion. It has been the subject of a 250K euros grant from Linksium, the French incubator for the Grenoble region: the technology start-up Picus Logica, of which I am a co-founder, is scheduled for launch in Q4 2017.

The three most important outcomes/results of the research activity of the candidate accompanied by the tangible and verifiable evidence that the presented results:

- are original, significant and due to the determining, prevailing and clearly recognizable contribution of the candidate;
- have been widely spread and have obtained outstanding recognitions by the international scientific community;
- qualify the candidate as a distinguished international expert in his/her own field.

1.2 List of the submitted publications (with a maximum number of 20) in addition to those listed at point 1.1. For each publication and/or set of publications, the candidate is required to briefly describe his/her contribution, their scientific/technical significance and individual importance, the overall impact of the results in the international scientific community.

These papers extend the concepts of paper [3] of section 1.1

[1] Portolan M., "Accessing 1687 systems using arbitrary protocols",2016 IEEE International Test Conference (ITC),Year: 2016, Pages: 1 - 9, DOI: 10.1109/TEST.2016.7805839

The flexibility of the new flow is used to propose an extension mechanism to support arbitrary protocols. So far, this is the first and only proposal in this space, and it is currenty under investigation for inclusion in the P1687.1 Working Group.

[2] M. Portolan, M. J. Barragan, R.Alhakim, S. Mir, "Mixed-signal BIST computation offloading using IEEE 1687", 2017 22nd IEEE European Test Symposium (ETS), Year: 2017, Pages: 1 - 2, DOI: 10.1109/ETS.2017.7968222

This paper shows the first working usage of 1687 to control mixed-signal instruments. Thanks to the new flow, it is possible to coordinate the execution of software routines and hardware instruments, opening new and exciting possibilities.

These papers (a Journal and a Conference) were published during the development of the IEEE 1687 standard. They were extremely important in raising the awareness of the need for a new language for the future standard by pointing of the description needs and the shortcomings of the

existing solutions such as CTL and BSDL. They had a deep impact on the development of 1687's languages ICL and PDL, which share several features with the "NSDL" proposed in the papers.

[3] Portolan M., Goyal S., Van Treuren B., Chiang C_H., Chakraborty T. and Cook T.B., « A Common Language Framework for Next-Generation Embedded Testing » IEEE Design & Test of Computers Volume: 27 , Issue: 5 , Pp: 36 – 49, 2010

[4] Portolan M., Goyal S., Van Treuren B., Chiang C_H., Chakraborty T. and Cook T.B., « A New Language Approach for IJTAG», 2008 International Test Conference (ITC08), San Francisco CA, October 26-30 2008

These two papers propose out-of-the box approaches for digital testing, with a significance advance over the field. For instance, the idea of using packetized approaches for high-speed access to JTAG is part of the IEEE 1149.10 standard, published in 2017. Similarly, the need of securing access to scan chain is now a hot topic, and [6] predates the work of Dworak and Crouch, now a reference in the field, by almost 5 years.

[5] Portolan M., « Packet-based JTAG for remote testing », 2012 International Test Conference (ITC12), Anaheim CA, 4-9 November 2012

[6] Portolan M., Goyal S. and Van Treuren B., « Scan chain Securization through Open-circuit Deadlocks », Poster for the 2010 International Test Conference (ITC10), Austin TX, November 2010

These papers come from the work of a PhD student I co-advised, Kais Chibani. In this work, We showed how it is possible to obtain relevant information about the sensibility of digital circuits to transient faults by RTL-level evaluation, with significant speed-up over traditional approaches like fault injection. This work is now the basis of a collaboration with the LIRMM laboratory in Montpellier, France, and it is also the subject of an industrial transfer with a big actor in the aeronautical field. My main contribution was in guiding the work and propose strategies to solve the high-complexity software issues, exploiting the expertise I gained in the Leon architecture during my previous work experience.

[7] K. Chibani; M. Portolan; R. Leveugle, "Evaluating application-aware soft error effects in digital circuits without fault injections or probabilistic computations", 2016 IEEE 22nd International Symposium on On-Line Testing and Robust System Design (IOLTS),Year: 2016, Pages: 54 - 59, DOI: 10.1109/IOLTS.2016.7604672

[8] K Chibani,, M Portolan, R Leveugle,, "Application-aware soft error sensitivity evaluation without fault injections-Application to Leon3", European Conference on Radiation and its Effects on Components and Systems (RADECS'16), 2016

[9] K Chibani, M Ben-Jrad, M Portolan, R Leveugle,, "Fast accurate evaluation of register lifetime and criticality in a pipelined microprocessor", Very Large Scale Integration (VLSI-SoC), 2014 22nd International Conference on, October

[10] K. Chibani, M Portolan, R Leveugle, "Fast register criticality evaluation in a SPARC microprocessor", Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph. D. Research in, June 2014

1.3 Complete list of all the significant publications of the candidate, including those listed at points 1.1 and 1.2 (to be attached to the end of the Curriculum).

2. Coordination of research and technology transfer groups and projects.

- Principal Inventor of 20 USPTO patent applications. 15 Granted as of September 2017. Between 2007 and 2010 I had the highest patent deposit ratio in Bell Labs Ireland.
- Responsible for the start-up maturation project "MAST", funded by the Linksium incubator in 2016-2017 for ~250k Euro.

- Co-founder and acting CTO of the resulting “Picus Logica” Start-Up, scheduled for launch in Q4 2017.

3. National and international reputation and professional activity for the scientific community

- Member of the IEEE 1687-2014 Standard Working Group from 2007 to its approval.
- Active member of the IEEE P1687.1 and “System JTAG” working groups

- Invited Talks;
    - Anghel L., Portolan M., “Managing Wear out and Variability Monitors: IEEE 1687 to the Rescue”, Keynote talk, East West Design and test Symposium, Yerevan, ARMENIA, 13 au 16 octobre 2016
    - Portolan M., “System Level Coordination of Multiple-Standard DfT”, Invited Talk, Test Standards Application Workshop (TESTA’16), Amsterdam, NETHERLANDS, 28 mai 2016
    - Portolan M., Standards: “Can they co-exist for System Level Test?”, Invited Talk, VLSI Test Symposium, Las Vegas, USA, 2016
    - Portolan M., “Flexible and Extendable System-level JTAG Manager”, International Test Conference 2015, USA.

- Global Coordinator of the TTTC « E.J. McCluskey Best Doctoral Thesis Award » since 2013
    - In this role, I was responsible of setting up the current format with the appointment of “local coordinators” who organize the semi-finals at the main Test events of each geographical area (ETS for Europe, VTS for North America, LATS for South America and ATS four Asia and Oceania), while I organize the final in ITC. This format allowed a better integrations of the semi-finals with the hosting conferences, with significant gains in organization stability and in the quality of the candidates.

- Vice General Chair for the « 2ndTest Standards Application Workshop (TESTA) », 2017
- Organiser of the « 1st International Test Standards Application Workshop (TESTA) », 2016
- « Awards co-Chair » for the « Test Technology Technical Council» (TTTC) since 2012
- « Industrial Liaison co-Chair » for the « 2012 European Testing Symposium » (ETS12), Annecy, France, 2012
- « Peer Reviewer » international conferences (ITC, ETS,IVLSI) and journals (IEEE Design and Test, Journal of Electronic Testing : Theory and Applications »)
- « Publication Chair » for the « 12th International On-Line Testing Symposium » (IOLTS06), Como, Italie, July 2006
- « Audio-visual Chair » for the « 11th International On-Line Testing Symposium » (IOLTS05), Saint Raphael, France, 2005
- Part of the review process for the « 10th International On-Line Testing Symposium » (IOLTS04), Madeira, Portugal, 2004

If the candidate has obtained the National Scientific Qualification in more than one Academic Field this must be considered a qualifying element, for properly evaluating the scientific reputation of the candidate.

- 2012: Obtained the French National Scientific Qualification for
    - Section 27 : Computer Science (“Informatique”)

- Section 61: Computer Engineering, Automatic Control and Signal Processing (“Génie informatique, Automatique et Traitement du Signal") :
- Section 63 : Electrical Engineering, Electronics, Photonics and Systems(« Génie électrique, électronique, photonique et systèmes »)

- 2006: Obtained the French National Scientific Qualification for
  - Section 61: Computer Engineering, Automatic Control and Signal Processing (“Génie informatique, Automatique et Traitement du Signal") :
  - Section 63 : Electrical Engineering, Electronics, Photonics and Systems(« Génie électrique, électronique, photonique et systèmes »)

4. Teaching activity

- Formal responsibility of Bachelor’s and Master of Science’s degree courses in Italian and/or foreign universities.
- Formal responsibility of Specializing Master’s courses and Life Learning courses in Italian and/or foreign universities in PhD courses.

FOREWORD: Grenoble-INP follows the French ‘Grand Ecole’ 2+3 format: students integrate the school after two years of Preparatory School and a national selection exam. The cursus takes 3 years and results in the delivery of a Specializing Master’s Degree (Diplôme d’Ingénieur), without formal intermediate Bachelor and Master Degrees. After a first common year, students are assigned to 2 years’ specialization courses (“filière”). My main teaching responsibilities are in these last two years of two filières:

- Filière “Embedded Systems and Software” (“Systèmes et Logiciels Emarqué”) : this option is common with the ENSIMAG School of Computer Science. This means half of the students and of the teachers come from each school in order to offer a curriculum where Electronics and Computer Science have an equivalent role.
  - “Intégration des Systèmes” (System Integration): this 2nd year class is composed by a theoretical half of 16,5 hours and practical lab experience for 33h. It is the main Electronics Design class for SLE, and gives the students an introduction to the concepts of Digital Design and Validation, with a special emphasis on VHDL. In the lab parts, students are asked to design a digital FIT filter control FSM in VHDL starting for high level specification. During the 8 sessions, they go through all the steps of RTL design: FSM definition, VHDL compilation and simulation, validation, synthesis and Place&Route on an ASIC target by exploiting industry standard tools from the main vendors (Mentor, Synopsys and Cadence).
  - Tolérance aux fautes (Fault Tolerance): this 3rd year class, composed of 18 hours of theoretical course and some practical exercises, presents students with the issues of fault tolerance in embedded systems and dependable design. Starting from an overview of the main origins of faults, the course presents the main approaches for Tolerance (Spatial, Temporal and Information Redundancy) for both hardware and software abstraction levels. 18h
  - “Etude de cas d'implantation d'un SLE" (Case Study of the implementation of an Embedded System) : this 3rd Year course is in fact a semester-long (48h) project where students work in groups of two or three to realize a complete prototype of a representative Embedded Systems proposed by one of the teachers. It is one of the flagship courses of SLE, and I have been part of the teacher’s pool since 2013 (the

responsible is Régis Leveugle), and proposed several subjects such as: “DPA attack on an ARM processor running Linux”, “Gameboy Emulator on a Xilinx FPGA”, “Secure Multimedia server of a Zynq FPGA”, “Virtual-machine based Fault Injection platform”, etc…

- Filière “Integrated Systems Design” (“Conception des Systèmes Intégrés”) : it is the first “Double Course” option opened by Phelma in 2013, where the students divide their time between academic classes and work a “apprentices” in enterprises in the Grenoble area (like, for instance, ST Microelectronics, Asygn or E2V).
    - “Projet conception” (Electronics Design Project) in this semester-long (84h) 2nd year project, the whole class (roughly 16 students) have to develop a Zygbee transmission system, starting from the system-level analysis to the design of the analog and digital blocks. At the end of the project (late June), the students are supposed to provide the GDSII files of their system, which is then sent to the CMP (http://cmp.imag.fr/) for production during summer. The chips are then used in the 3rd year for the test and Characterization labs. It is an extremely rare opportunity for students to have their design actually fabricated.
      In this project, I am co-responsible for the Digital part to guide and help the students specify, implement and validate their blocks following industrial quality guidelines and methods in order to obtain valid GDSII files.
    - “Projet informatique” (Computer Science Project). In this 2nd year 30h project, the CSI students are faced with a true challenging project: the specification and implementation of a VHDL synthesis tool in C/C++. It is the opportunity for electronics-oriented students to get the Computer Science skills whose importance is rapidly increasing in the working world. This class was created from scratch together with my colleague and co-responsible Katell Morin-Allory.
    - “Analyse et réalisation d'un système complexe » ("Analysis and Implementation of a complex system) : this 52h 3rd year project is inspired from the above-mentioned ““Etude de cas d'implantation d'un SLE" and follows the same format. I am part of the teacher’s pool (the responsible is Lorena Anghel) and I proposed subject such as “VHDL/ARM hybrid controller for robotics on a Zynq Plateform” or “RISC-V based secure system”.
    - “Test des circuits conçus en 2A” (Test of the circuits implemented in the 2nd year) : in this 24h lab class, I am responsible for the Digital part (12h). The students have the opportunity to test their own circuits by appling APTG patterns thanks to a Phelma-developed FPGA-based digital tester. In the event of the circuits not being available (typically because of problems/errors during design), some off-the-shelf circuits are used for the lab.

- Formal responsibility of PhD courses in Italian and/or foreign universities.
    - Since 2013, I propose together with Salvador Mir, the Director of TIMA Lab, an introductory class to Test for the PhD students of Grenoble’s Doctoral School EEATS (edeeats.grenoble-inp.fr). In two 4h sessions I given an introduction to the main issues of Digital Test and Design for Test, with a special emphasis on the open research problems, while Salvador focuses on Analog and Mixed-Signal test.

5. Institutional offices and roles in Italian and foreign Universities and/or public and private institutions with scientific and/or technology transfer aims

- Since 2014 I am the responsible for Phelma for the filière “Embedded Systems and Software” (“Systèmes et Logiciels Emarqué”) : this option is common with the ENSIMAG School of Computer Science. This means half of the students and of the teachers come from each school in order to offer a curriculum where Electronics and Computer Science are mixed. My role as a responsible has been to coordinate the communication between the two schools, to advise and guide students and compose the didactic offer together with my ENSIMAG counterpart. In particular, we had to assure an internal reform to move towards the Bologna Process, which is extremely different from the traditional French “Grand Ecole” format G-INP follows. This required in the first stage to re-arrange the whole SLE offer into coherent Units of 6 ECTS. The second stage, still ongoing, is transitioning from a year-based validation process to Bologna’s Unit-based. This implies a profound transformation of G-INP methods, whose consequences are not still completely known: a responsible, my role it to help and survey this transformation to assure the quality standards of our university are guaranteed.
- In 2016, I was one of the actors of the fusion between SLE and ISSC (Internet, Services and Connected Systems), the other commons option between Phelma and ENSIMAG. This resulted in the creation of the new option SEOC (“Systèmes Embarqués et Object Connectés”, “Embedded Systems and Connected Objects), which will start in September 2017. The idea is to add Networking and Communications to the core skills of SLE to better prepare the students for the new challenges opened, for instance, by the Internet of Things or Communicating Objects. The option received a warm welcome from students and colleagues alike, and raised a significant interest from G-INP industry partners.
- In 2013-2017, I worked in close relationships with Said Obbade, Phelma Responsible of Enterprise Relationships to strengthen our bonds with Freescale/NXP, which resulted in June 2017 in the signing of a long-term Partnerships Agreement. My role was to provide NXP with information about our curricola and to help promoting NXP with our colleagues and students. I was notably responsible for having Phelma participate in the Freescale/NXP cup, their flagship University program, with extremely positive results (Phelma qualifies to the Europe finals three times out of three participations).

Place and date _____

Full Publications List

International Journals

[J.1] Portolan M., Goyal S., Van Treuren B.,, «Executing IJTAG: Are Vectors Enough? » Design & Test, IEEE , vol.30, no.5, pp.15,25, Oct. 2013

[J.2] Portolan M., Goyal S., Van Treuren B., Chiang C_H., Chakraborty T. and Cook T.B., « A Common Language Framework for Next-Generation Embedded Testing » IEEE Design & Test of Computers Volume: 27 , Issue: 5 , Pp: 36 – 49, 2010

[J.3] Portolan M., Leveugle R., « A Highly Flexible Hardened RTL Processor Core Based on LEON », IEEE Transactions on Nuclear Science, Volume 53, Issue 4, Part 1, Aug. 2006 Page(s):2069 - 2075

Internationals Conferences

[C.1] M. Portolan, M. J. Barragan, R.Alhakim, S. Mir, "Mixed-signal BIST computation offloading using IEEE 1687", 2017 22nd IEEE European Test Symposium (ETS), Year: 2017, Pages: 1 - 2, DOI: 10.1109/ETS.2017.7968222

[C.2] Portolan M., "Accessing 1687 systems using arbitrary protocols",2016 IEEE International Test Conference (ITC),Year: 2016, Pages: 1 - 9, DOI: 10.1109/TEST.2016.7805839

[C.3] K. Chibani; M. Portolan; R. Leveugle, "Evaluating application-aware soft error effects in digital circuits without fault injections or probabilistic computations", 2016 IEEE 22nd International Symposium on On-Line Testing and Robust System Design (IOLTS),Year: 2016, Pages: 54 - 59, DOI: 10.1109/IOLTS.2016.7604672

[C.4] M. Portolan, R. Rolland, "Student-driven development of a digital tester", 2016 11th European Workshop on Microelectronics Education (EWME), Year: 2016, Pages: 1 - 3, DOI: 10.1109/EWME.2016.7496479

[C.5] K Chibani,, M Portolan, R Leveugle,, "Application-aware soft error sensitivity evaluation without fault injections-Application to Leon3", European Conference on Radiation and its Effects on Components and Systems (RADECS'16), 2016

[C.6] Portolan M., "A novel test generation and application flow for functional access to IEEE 1687 instruments", 21th IEEE European Test Symposium (ETS), Year: 2016, Pages: 1 - 6, DOI: 10.1109/ETS.2016.7519302

[C.7] K Chibani, M Ben-Jrad, M Portolan, R Leveugle,, "Fast accurate evaluation of register lifetime and criticality in a pipelined microprocessor", Very Large Scale Integration (VLSI-SoC), 2014 22nd International Conference on, October

[C.8] K. Chibani, M Portolan, R Leveugle, "Fast register criticality evaluation in a SPARC microprocessor", Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph. D. Research in, June 2014

[C.9] Portolan M., « Packet-based JTAG for remote testing », 2012 International Test Conference (ITC12), Anaheim CA, 4-9 November 2012

[C.10] Portolan M., Goyal S. and Van Treuren B., « Scan chain Securization through Open-circuit Deadlocks », Poster for the 2010 International Test Conference (ITC10), Austin TX, November 2010

[C.11] Portolan M., Goyal S. and Van Treuren B., « Integrated Architecture for Scalable Testing», Poster for the 2009 International Test Conference (ITC09), Austin TX, November 2009

[C.12] Vanhauwaert, P.; Portolan, M.; Leveugle, R.; Roche, P., « Usefulness and effectiveness of HW and SW protection mechanisms in a processor-based system», 15th IEEE International Conference on (ICECS 2008), Electronics, Circuits and Systems, 2008

[C.13] Portolan M., Goyal S., Van Treuren B., Chiang C_H., Chakraborty T. and Cook T.B., « A New Language Approach for IJTAG», 2008 International Test Conference (ITC08), San Francisco CA, October 26-30 2008

[C.14] Portolan M., Leveugle R., « A Highly Flexible Hardened RTL Processor Core Based on LEON », 8th European Conference on Radiation and Its Effects on Components and Systems (RADECS 05) – 2005

[C.15] Portolan M., Leveugle R., « Towards a Secure and Reliable System » – 2005 IFIP International Conference on Embedded and Ubiquitous Computing (EUC'2005) – 2005

[C.16] Portolan M., Leveugle R., « On The Need for Common Evaluation Methods for Fault Tolerance Costs in Microprocessors » Proceedings of the 11th International On-Line Testing Symposyum (IOLTS05) – 2005

[C.17] Portolan M., Leveugle R., « Operating systems function Reuse to achieve Low-Cost Fault-Tolerance », 10th International On-Line Testing Symposyum (IOLTS04) – 2004

[C.18] Portolan M., Leveugle R., « A Context-Switch Based checkpoint And Rollback Scheme » – Proceedings of the XIX Conference on Design of Circuits and Integrated Systems (DCIS 04) – 2004

Workshops

[W.1]M. Portolan, M. J. Barragan, H. Malloug, S. Mir, "Interactive Mixed-Signal Testing Through 1687", First International Test Standards Application Workshop (TESTA'16)

[W.2][W.1] Portolan M., Goyal S., Van Treuren B. « A New Execution Model for Interactive JTAG Applications », 2013 European Test Symposium (ETS13), Avignon, France, May 2013

[W.3][W.2] Cherubini D., Portolan M., "Automatic Equivalent Model Generation and Evolution for Small Cell Networks" Fourth International Workshop on Indoor and Outdoor Small Cells 2013 (WiOPT), Tsukuba, Japan, Mai 2013

[W.4][W.3] Portolan M., Goyal S., Van Treuren B., Chiang C_H., Chakraborty T. and Cook T.B., « A new description language for SoC testing », 2008 European Test Symposium (ETS08), Verbania, Italy, May 25-29, 2008

[W.5][W.4] Portolan M., Goyal S., Van Treuren B., Chiang C_H., Chakraborty T. and Cook T.B., « A Novel Hardware Description language for efficient debug and diagnosis of digital circuits », 2008 IEEE International Workshop on Silicon Debug and Diagnosis (SDD2008), San Diego, CA , April 27- May 1st, 2008

National Conferences

[C.n.1] Portolan M., Leveugle R., « Réalisation d'une Tolérance aux Fautes à Bas Coût dans les SoCs en Utilisant le Système d'Exploitation » – Actes des Journées Nationales du Réseau Doctoral de Microélectronique - 2004

Patents

Granted (Test)

1. “Method And Apparatus For Describing And Testing A System-On-Chip”, Chakraborty 12-4-12-1-10 08), , US Patent 7,958,479, June 2011 (EU patent 2232373)
2. “Method And Apparatus For Describing Components Adapted For Dynamically Modifying A Scan Path For System-On-Chip Testing”, US Patent 7,962,885 June 2011
3. “Method And Apparatus For Describing Parallel Access To A System-On-Chip”, US Patent 7,949,915 May 2011 (EU patent 2232372, KR patent 101121306)
4. “Apparatus And Method For Isolating Portions Of A Scan Path Of A System-On-Chip”, US Patent 7,958,417 June 2011
5. “Apparatus And Method For Controlling Dynamic Modification Of A Scan Path”, US Patent ,7,954,022 May 2011
6. “Method And Apparatus For Providing Scan Chain Security”, Michele Portolan, Suresh Goyal , Bradford Van Treuren, US Patent 8,495,758 July 2013
7. “Method And Apparatus For System Testing Using Multiple Instruction Types”, Michele Portolan, Suresh Goyal , Bradford Van Treuren, US Patent 8,533,545, September 2013
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